Multimedia, not just graphics, display capability

By Manish Singh

Robust multimedia content not only requires fast, high-resolution displays, but also calls for relatively new capabilities such as secure transmission of rights-managed audio and video streams. DisplayPort, with a new specification version recently approved by VESA, seeks to redefine the display interface for more robust functionality.

GRAPHICS DISPLAY GLOSSARY	
AUX CH	Auxiliary Channel
DVI	Digital Visual Interface
EDID	Extended Display Identification Data
HDCP	High-bandwidth Digital Content Protection
HPD	Hot-Plug Detect
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential SCSI
RGB	Red, Green, Blue
VESA	Video Electronics Standards Association

The PC and consumer electronics industries continue to demand increased LCD resolution, color depth, and higher refresh rates driven by their desire to deliver immersive, high-quality, high-resolution video and gaming experiences. This, in turn, creates the demand for a high-bandwidth, scalable, display interconnect standard. As PCs integrate high-definition DVD playback and support Internet-based HD video services, digital interconnect technology is needed to securely transmit copyrighted audio and video streams to high-resolution displays.

Legacy display interface technologies have several limitations. These restrictions include the necessary bandwidth capacity to scale to higher resolutions and color depths, as well as cable length and content protection limitations, all of which raise concerns about the interface technologies' viability for future use. Existing standards also add complexity by requiring voltage translations, resulting in additional processing and cost. These requirements indicate that PCs must often support multiple display interconnect standards, which add to system complexity and cost. Clearly, the PC and consumer electronics industries need a single standard that can support future needs based on a new set of technologies.

DisplayPort, an extensible digital display interconnect standard adopted by VESA, overcomes current standards' limitations by accommodating new display features and applications. DisplayPort aims to reduce device and system design complexity and to provide performance scalability for next-generation LCDs. To that end, DisplayPort is an open, industry-standard, digital interface developed for a wide range of applications. The DisplayPort specification defines a scalable, digital display interface with optional audio and content protection capability for various applications. DisplayPort supports both external (box-to-box) and internal (chip-to-chip) connections.

DisplayPort overview

Sink functionality is defined as the capability to support the reception of a DisplayPort stream, such as shown in Figure 1. A Sink device contains one sink function and at least one rendering function. *Rendering* is the function of displaying or processing stream data. For example, video displays and speakers are considered rendering functions. *Source functionality* is defined as the capability to transmit a DisplayPort stream. A Source device contains one or more source functions.

Branch devices are located between Source and Sink devices. Some examples of branch devices include:

- Repeater (one DisplayPort in, one DisplayPort out)
- Replicator (one DisplayPort in, multiple DisplayPorts out)
- Concentrator (multiple DisplayPorts in, one DisplayPort out)

To support the market as it transitions from legacy standards to DisplayPort, the standard defines two additional branch devices – legacy-to-DisplayPort converter and DisplayPort-to-legacy converter.

Layered architecture

DisplayPort, based on a layered architecture as shown in Figure 2, consists of the Policy Maker Layer, Link Layer, and Physical Layer.

The DisplayPort Physical Layer link consists of the Main Link, AUX CH, and HPD signal line. The Main Link provides a scalable, forward drive channel and implements a micropacket architecture that can support variable color depths, refresh rates, and display resolutions. AUX CH is a bidirectional return channel that also implements micropacket architecture for flexible control and status information delivery.

The layered architecture decouples the Physical Layer evolution from the Link Layer such that future enhancements to the Physical Layer can be supported seamlessly, thus adding to DisplayPort's extensibility.

Policy Maker Layer

The Policy Maker Layer manages data streams and the link. The standard is flexible about its implementation.

Link Layer

The Link Layer manages the isochronous transport and link device services. Isochronous transport services in a Source device map the audio and video streams into the Main Link such that streams can be reconstructed properly by the Sink device. Link service is used for discovering, configuring,

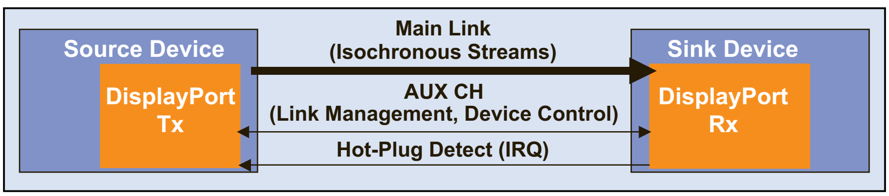

Figure 1

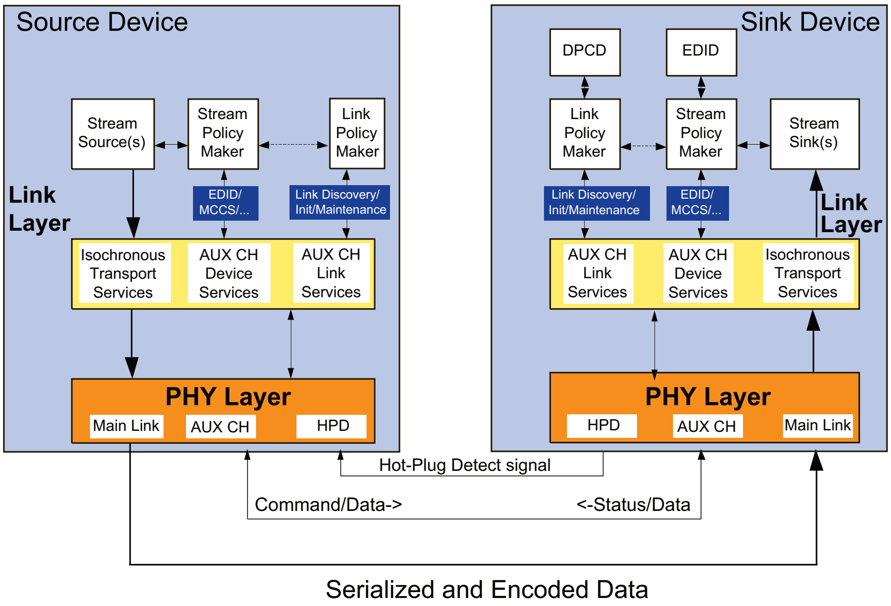

Figure 2

and maintaining the link by accessing the Sink device's DisplayPort configuration data over AUX CH. The device service supports device-level applications such as EDID access and monitor control command set over the AUX CH.

At the Link Layer level, both the Main Link and AUX channel support a micro-packet architecture in which data streams are packed into transfer units. These transfer units are then mapped to the Main Link or AUX link. In addition to enabling support for variable color depths, refresh rates, and display pixel formats, this architecture enables DisplayPort to extend its functionality to adopt new data types and thus new features for legacy and emerging applications, adding another dimension to DisplayPort's scalability.

Physical Layer

The Physical Layer comprises the Main Link, AUX CH, and HPD signal. The logical functions supported at this layer include scrambling/descrambling and ANSI 8B/10B/Manchester II encoding/decoding. SERDES, differential current driving/receiving, and preemphasis/equalization functions are supported at the electrical level.

Main Link

The Main Link is a unidirectional, high-bandwidth, low-latency channel used for transporting isochronous streams such as uncompressed video and audio. The Main Link consists of AC-coupled, doubly terminated differential pairs called *lanes* and can be scaled from one to four lanes.

The standard supports two link rates: 2.7 Gbps and 1.62 Gbps per lane. The link rate is decoupled from the pixel rate, which is regenerated from the link symbol clock. The capabilities of the DisplayPort transmitter and receiver and the quality of the channel (that is, a cable) will determine whether the link rate is set to 2.7 Gbps or 1.62 Gbps per lane.

The Main Link has one, two, or four lanes. The number of lanes is decoupled from the pixel bit depth (bits per pixel) and component bit depth (bits per component). Component bit depths of 6, 8, 10, 12, and 16 are supported with the colorimetric RGB and YCbCr444/422 formats, regardless of the number of Main Link lanes.

All lanes carry data, and there is no dedicated channel for the forwarding clock. The link clock is extracted from the data stream encoded with ANSI 8B/10B coding rule (specified in ANSI X3.230-1994, clause 11).

Excluding the 20 percent channel-coding overhead, DisplayPort's Main Link provides for the application bandwidth (also called link symbol rate) as shown:

Link rate = 2.7 Gbps

- One lane = 270 MBps
- Two lanes = 540 MBps
- Four lanes = 1,080 MBps

DisplayPort devices may freely trade pixel bit depths with the resolution and frame rate of a stream within the available bandwidth. Audio and other secondary data packets may be transported during the main video stream's horizontal and vertical blanking period.

AUX CH

A half-duplex, bidirectional channel used for link management and device control, AUX CH consists of an AC-coupled, doubly terminated differential pair. Manchester II coding is used as the channel coding for AUX CH. As is the case with the Main Link, the clock is extracted from the data stream. AUX CH transaction starts with synchronization transmission.

AUX CH is a low-latency interface with a transaction period of < 500 µs. It provides for 1 Mbps of data rate over the supported cable lengths. AUX CH syntax is defined in a way that seamlessly supports I2C transaction over AUX CH.

The HPD signal also serves as an interrupt request by the Sink device. This signal is used to notify the connection of a Sink device and the Source device of any change in link status.

Channel coding and device support

DisplayPort precludes a dedicated clock channel to minimize clock-related EMI. In addition, the clock and data are scrambled and then encoded in the ANSI 8B/10B (Main Link) or Manchester II (AUX CH) format, further minimizing EMI. DisplayPort Sink devices support link frequency down spreading to further reduce EMI, which is optional in Source devices. Alternative display interconnect standards do not provide such a comprehensive framework for mitigating EMI as effectively.

The DisplayPort interface is AC coupled, enabling the Source and Sink devices to support independent common mode voltage such that each IC can be implemented in the process technology best suited to the application requirements. For example, graphics processors can be implemented in a 65 nm process while timing controllers can be implemented in 350 nm and still interface seamlessly. LVDS and DVI standards lack this capability.

Unlike DVI and LVDS, DisplayPort natively supports secure audio data transmission. This is key for the new generation of multifunction monitors targeted at video and gaming applications.

DisplayPort incorporates the HDCP version 1.3 standard for securing copyprotected content. This is an important feature for PCs that are becoming multimedia hubs used for playback of high-resolution, premium content like HD movies.

Mechanical features

The DisplayPort specification also includes a mechanical specification that defines a small, external connector with an optional latch on the plug for robust connectivity with long cable lengths. Figure 3 shows a DisplayPort cable and connector. DisplayPort-compliant Source and Sink devices will interoperate over a 15-meter cable-connector assembly. The connector, which is optimized for use on thin profile notebooks, includes four forward lanes and allows up to four connectors on a graphics card. A standard panel connector for internal applications is also defined within the mechanical section of the specification. In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-legacy converter.

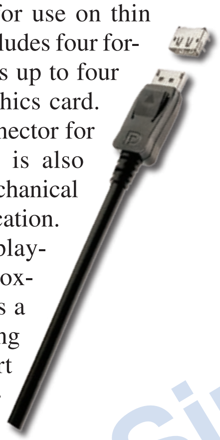

Figure 3

Innovation through collaboration

VESA is one of the PC industry's most influential sources of display-related standards. The organization, which has 145 member companies including representatives from every part of the PC ecosystem, has launched more than 60 standards in display-related fields. VESA's objective in developing DisplayPort was to enable members of the display industry to influence and contribute to its specification. Unlike closed, proprietary standards, DisplayPort provides a fair, open standard approval process that solicits input from all VESA members. This enables broad adoption and initiates a cycle of innovation through collaboration. VESA members approved DisplayPort Version 1.1 in April 2007.

Companies within both the PC and consumer electronics industries recognize DisplayPort's unique capabilities as an open standard that comprehensively serves their demands by providing a high-bandwidth, scalable, and secure digital interface for chip-to-chip or box-to-box connectivity.

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