

Interpolating DACs offer high speeds, but are they controllable?

By Scott Hames



Current state-of-the-art software defined radio transmit techniques typically involve synthesis of signals at the Intermediate Frequency (IF) or, even in some cases, such as High Frequency (HF) and Very High Frequency (VHF), at the Radio Frequency (RF). Such synthesis demands data streaming to the Digital Analog Converter (DAC) input at very high rates, approaching 1 GHz in some cases. Supplying data at these rates is a serious challenge, even between components on the same board. To alleviate the problems of moving data at high speed and simplifying system design, DAC manufacturers are offering parts that include on-chip clock multipliers, Direct Digital Synthesis Numerically Controlled Oscillators (DDS/NCOs), interpolating filters, and mixers. The theory is that by digitally performing the final upconversion on the DAC chip, the user need only supply data at the baseband rate. Furthermore, the programmable NCO can bring substantial flexibility to the hardware, enabling software control for spread spectrum techniques such as frequency hopping. While these features provide obvious benefits, there are subtle caveats that should be noted when specifying DACs for phase-sensitive applications.

Experimenting with digital upconverter DACs

Phased array radar is a prime example of a phase-sensitive application that requires exact synchronization of multiple DAC outputs across multiple trigger events. In the past, it was commonplace to use “standard” DACs – simple but fast devices that enabled clock and data input control. However, the problem was ensuring clock and data stream synchronization. As DAC conversion rates increased beyond about 300 MHz, keeping the clock and data rates down to manageable levels drove experimentation with what could be called *interpolating* or *digital upconverter DACs* – devices that accept data at the baseband rate, and then perform Digital UpConversion (DUC) functions on the chip, before generating the analog output. Unfortunately, in most cases, the user is limited in precisely con-

trolling the internal DUC functions of these parts. This limitation eliminates the possibility of ensuring that the outputs are truly synchronous. In many applications, they do more harm than good.

At ICS, we have performed an extended evaluation of a particular 200 MHz interpolating DAC – but have had to abandon the effort. The DAC in question includes all the features previously listed, including an on-chip clock multiplier, DDS NCO, interpolating filters, and mixers. Although it has been very successful in some applications, it has been a total failure in phase-sensitive situations. One target application was generating a radar system FM chirp pulse. It was critical that the phase and timing of the output be the same (sub-nanosecond consistency) from one trigger to the next, and across multiple channels. Also, the ability to set phase

arbitrarily across channels for transmit beam forming was highly desirable, if possible.

The need for user control

Because the DAC in question was operating as a quadrature upconverter, it relied on an internal DDS NCO. This operation produced the intermediate frequency for modulation by the incoming data. The phase of any signal generated at the DAC output would depend on the phase of the baseband data and the phase of the DDS NCO. Unfortunately, even if the onboard logic perfectly controlled the input data timing, the NCO was free running after chip release from the reset condition. The user could not reset the phase of the NCO to zero, or any other known point, on demand. Ideally, the requirement was to use the variable Pulse Repetition Interval (PRI) trigger input to restart the NCO, so that every pulse was identical. Two necessary features that simply did not exist were:

- A register in the chip that would allow specification of the starting phase of the DDS NCO
- An NCO_SYNC pin on the device that would clear the phase accumulator and allow arbitrary synchronization based on an external event

Difficulties with synchronization

On-chip clock multipliers are another feature that adds risk to phase-sensitive multichannel designs. Many high-speed DACs accept a low-speed clock and multiply it up to a much higher speed internal clock. This process is risky because in multichannel systems, each chip usually generates its own high-speed inter-

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nal clock using a Phased Lock Loop (PLL). Since each PLL will lock up at a slightly different time after the clock is applied, changed, or the chips are reset, the DAC clocks will always be different. Furthermore, after the high-speed clock is generated, it is often contained within the chip, so that no other equipment, such as other DACs, can be synchronized with it. If there is to be a clock multiplier on chip, it is imperative that it has the ability to deliver the full-speed conversion clock to the outside world, not a low-speed derivative of it.

Other parts of the processing chain that will affect the phase of the signal are, for example, interpolation counters and Finite Impulse Response/Infinite Impulse Response/Cascaded Integrator Comb (FIR/IIR/CIC) filter pipelines. The state of the interpolation counter determines when new data is accepted into the pipeline. Unless the counter state can be controlled based on external conditions, phase uncertainty exists. In addition, if old, invalid data is not flushed from filter pipelines, it could corrupt the new input. Designers of phase-sensitive systems will want to ensure that they have access to all of these controls.

Solution built around GrayChip products

A solution that has worked was a separate DDC ASIC from GrayChip (now owned by Texas Instruments) that converted the baseband input data to the final intermediate frequency before feeding it to a standard DAC. The GrayChip 4116 and 5016 in particular were outstanding products, with an excellent implementation of all the features previously mentioned (DDS NCOs, interpolating filters, mixers) and more. A multilevel synchronization scheme enables internal or external synchronization of virtually every parameter in the signal processing chain. Although this scheme puts responsibility for proper control of the device squarely on the system designer or application programmer, and the learning curve is substantial, it is extremely powerful in the hands of an experienced user.

In summary, the high speeds offered by many of today’s interpolating DACs are

superficially attractive, but implementation in real-world applications requires a deep understanding of how they work and their limitations if the systems designer is to be able to take advantage of them.

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