

# PC/104: making room for greater performance

By Steve Potocny and Cliff Moon

*Today's x86 processors can indeed fit into PC/104 footprints with proper care and feeding. Kontron shares their perspective on working with past and present Intel processor technology within the limitations of PC/104 and calls for continued adaptation in the standard to embrace PCI Express (PCIe).*

Since the release of its first specification in 1992, the PC/104 form factor has been growing in popularity, with embedded systems architects continually pushing the limits of PC/104 designs. More than a decade ago, the technology presented challenges with regard to fitting Intel 486 processors – then much larger, slower, and consuming less power – onto a small board.

In contrast, the technology available today forces designers to be creative in populating the tight space with numerous small components, many of which consume far more power than the previous generations. As personal and industrial computing continues to raise the bar for users, embedded computing solutions are expected to operate at a similar level, incorporating the latest x86 processors for comparable graphics and data processing.

This can be daunting to a designer who now faces power-management challenges in addition to new mechanical, thermal, and electrical considerations. Incorporating the latest x86 processors and emerging bus types in PC/104 CPU boards offers tremendous potential for unprecedented performance, but many factors must be addressed in the initial design phase.

## Facing the wall

It is well known that no universal computing solution exists, but rather each application is accompanied with a unique set of system requirements. Thus, peripheral speed and bandwidth considerations are necessary throughout all stages of system design. Graphics applications today require more processing power than ever before, whereas data-intensive applications require greater bandwidth and lower latency. As processors such as Intel's Pentium D became faster and consequently hotter and more power-hungry, PC/104 designers ran into a wall of sorts. They could not take full advantage of the speed

and high level of relative performance such processors offered because they had no way to dissipate processor power on the small board or within the system.

At the same time, user demands continued to multiply along with the growth of embedded computing. Given consumers' increasing dependence on mobile electronics and the attention this has brought to hardware designers, it is foreseeable that mobile technology advancements will transfer to embedded computing. The range of system applications will continue to expand because designers will have more hardware options to include in compact systems.

## Thermal and mechanical considerations

Naturally, faster clock rates, graphics processing, and memory transfers increase switching and require more power. Hot operating environments lead to lower performance, making cooling a critical design consideration. In a race for the fastest processor in the Pentium D age, power consumption in some designs has risen to as much as 15 times the 8 W of popular 400 MHz processors. In addition to hot processors, it has been notably difficult to control graphics chips' thermal behavior. The dilemma of cooling both of these large, older components, especially those with less efficient power consumption, has been compounded with the 0.6" height requirement of PC/104. An example of a Pentium M PC/104-Plus SBC, the Kontron MOPS-PM, is pictured in Figure 1.

Passive cooling has not provided an adequate solution in most cases, and active cooling methods have continued to evolve and address the thermal challenges of PC/104 systems. Advanced Configuration and Power Interface (ACPI) has provided the industry with guidance to power management, which has been improved

independently. Many processors feature thermal diodes, thermistors, or thermocouples in addition to thermal control circuitry, detecting temperature variations and reacting before the system degrades or overheats. Instead of simply shutting down or slowing, newer processors support sophisticated algorithms in an effort to dynamically change the chip's thermal behavior. It is desirable that this operation be transparent to the user, maintaining a comparable level of system performance and noise.

When designing a system, it is important to consider the thermal and mechanical implications of each processor package type. Pin, land, and ball grid arrays have been standard during the past several years. Land grid arrays are more rugged prior to installation because the danger of bending or otherwise damaging a pin is transferred to the less expensive board, though this arrangement comes with the cost of operating temperature limitations. Pin arrays typically are composed of ceramic or thermally superior plastic.

Especially in the case of ball grid arrays, ensuring reliable contact between the chip and board as well as the chip and its cooling device can lead to more stringent board flatness requirements. As the environmental implications of manufacturing, assembly, and electronics use become more visible worldwide, RoHS has convinced many companies to eliminate lead-based solder and other harmful chemicals from use. This means the method of attachment for computing components will introduce additional variables to mechanical and thermal design considerations.

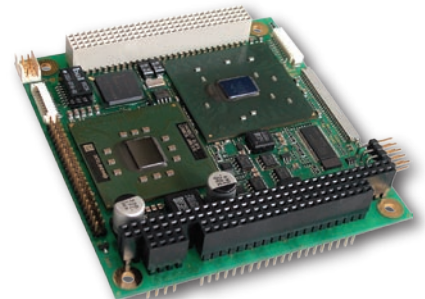


Figure 1

## Next wave: Intel Core 2 Duo

Processor designers have been hard at work to solve some of the problems faced by designers who want to push the envelope with unprecedented performance in small form factor systems. Pentium desktop processors required up to 130 W, an unmanageable figure for PC/104 and other similar form factors such as EPIC. The demand for reduced power and consistently improving performance in small packages is no longer unreasonable, but instead is recognized as an important factor in the definition of future computing and thus the parameters of processor design. Introduction of Intel's Core line of processors shifted the design goal from increasing clock rates to maximizing resource utilization efficiency. Much of the power reduction comes from integrating intelligent thermal control within the processor, as accomplished with SpeedStep in the earlier Pentium M processors. The result is a line of processors incredibly well suited for the embedded environment.

The Intel Core 2 Duo (Figure 2) at least halves the thermal footprint of the Pentium with new models achieving as low as 17 W with lower supply voltage and a reduced core speed option. Instead of remaining powered, an adaptive monitoring system allows voltage and core frequency to be adjusted dynamically. Power is only applied where it is necessary, and the frequency is adjusted to match the application requirements. In fact, the tremendous power savings from implementing such schemes result in a minimal loss of performance compared to previous designs that allowed for either maximal performance through maximal power or minimal power consumption that resulted in minimal performance.

The Core 2 Duo employs two thermal sensors that continually monitor each core's temperature and provide key inputs used by the power-management policies and chipset to set the fan speed. Processes can switch execution seamlessly between

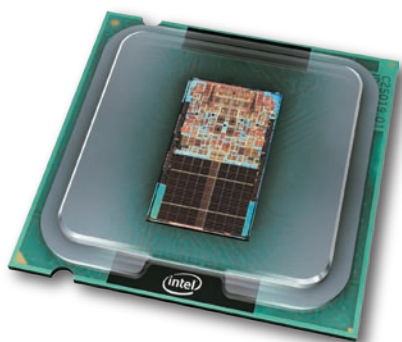


Figure 2

cores and run in a way that maintains uniformity in the chip temperature. This improvement in power utilization ensures optimal system performance and extends the processor's lifetime.

Multiple core processors can bring many advantages. Intel is introducing dual cores with its new 65 nm process, and quad cores are following quickly with 45 nm and smaller processes. These new processes allow for multiple cores to reside in the same size packages used by previous designs while making room for additional features. Board space is then free for more memory and other interfaces, potentially reducing the number of boards needed in a system.

In addition to being designed for multitasking and multithreading, today's processors have faster front side buses and can handle 128 bits of information at once, redefining computing capabilities for processor-intensive applications. Cache and memory management are implemented with maximal efficiency, pre-fetching data to a single location for use by either core. Designers may choose from a variety of chipsets for optimal performance in data- or graphics-intensive applications.

### PC/104 adaptability

Many designers have been tempted to stray from x86 in favor of custom processors that deliver more speed for less power. While that may be a solution for custom applications, the capabilities of the system remain only as good as the interface by which it operates. Whether overcoming the processor barrier with a custom solution or incorporating a powerhouse from the Intel Core product line, current drawbacks of PC/104, such as ISA and PCI bus interfaces' inherent speed limitations, must be addressed to balance the system design.

In 1992, PC/104 emerged with the ISA bus, providing 104 signals with a unique pin and socket stacking design that eliminated the need for a backplane. Development in peripherals and processors trended to PCI, so PC/104-Plus was created to provide an ISA-to-PCI bridge, enabling a PC/104 board to interface with both ISA and PCI boards. Further change was implemented in PCI-104 to eliminate the ISA bus entirely, thereby saving valuable board space for additional components with pure PCI interface.

PC/104 has been a popular form factor for use in environments that require rugged

hardware and high reliability for maximal uptime where repair or replacement may not be possible. Space constraints and suitability for low-power applications have created a niche for PC/104 in applications that would not require game-quality graphics processing, though that is by no means the extent to which the size of PC/104 makes it desirable. The military, aerospace, and medical industries are especially interested in using PC/104 systems in signal, image, and data-processing applications, particularly with real-time processing and data transfer.

At 33 MHz, the PCI bus lacks more than just speed. Data transfer does not provide for data synchronization or prioritization, thus subjecting important signals to bottlenecks on the bus, especially when there is more traffic than the bus is designed to support. A protocol other than PCI or ISA will be necessary to achieve this goal, and PC/104 is again called upon to incorporate changes that allow it to prevail as the form factor of choice.

With current processor capabilities and increasing peripheral demands within a system, PCIe has emerged as a strong competitor for the bus of choice. As it has done in the past, the PC/104 standard must adapt to provide competitive solutions for embedded system designs. Specifically, PC/104 must find a way to interface with the newer PCIe standard to match the bandwidth of the bus with the speed of the processor within a PC/104-based system.

### PCIe's potential

The PCIe 2.0 standard was released last fall, defining an even more powerful interface than that which helped the initial standard gain popularity so quickly. PCIe offers numerous solutions to the shortcomings of PCI. Most importantly, the new specification doubles the interconnect bit rate. This increase in bandwidth allows designers to reduce costs in implementing narrower interconnect links for greater performance. With a theoretical peak bandwidth of 16 GBps in a 16-lane system, it is clear what draws attention to the standard.

In addition to its speed, the methods for handling serial signals with parallel connections attract designers. Bits are not required to arrive simultaneously, alleviating the need for data synchronization. Prioritized data serves to avoid bottlenecks common in overloaded PCI systems. Handshaking and error detection ensure the integrity of each transfer,

which can be especially useful in the presence of noise.

PCIe has the added advantage of transparency to operating systems, making it fully backward compatible with PCI software. However, electrical modifications are required to interface PCI with PCIe. PC/104 has +5 V, -5 V, +12 V, and -12 V supplies, but PCIe uses two pairs of differential 2.5 V LVDS signals in each lane to transmit and receive on the bus. Novel connectors have been proposed for directly stacking PCIe I/O boards in a PC/104 system. Using PCIe as the base, PC/104 ISA cards can be stacked to create a system with a height of four.

PC/104 is working on a standard by which PCIe can be integrated in the long line of interfaces. Given the availability of a PCIe chipset in Intel's Core line, the prospect of encapsulating the two interfaces in a single standard makes PC/104 a candidate for applications beyond its current reach.

#### Still more room for innovation

PC/104 will remain a dominant form factor as long as its adaptability continues, embracing new features and processing technology so users can continue to advance performance and function in their applications.

Cooperation from processor innovators like Intel alleviates many barriers designers encountered, beginning with the Pentium processors and including others that compete in the race for speed. Mobile computing and portable consumer electronics have aided tremendously in this advancement because those markets demand smaller, faster devices with low power consumption realized through extended battery life. The shift toward maximizing resource efficiency within the processor and making chipsets more tailored to a particular application can only allow for the expansion of PC/104 form factor applications.

As processes shrink to 65 nm and less, locating even more features with the cores in the processor will become possible. With so many processor options available and the prospect of compatibility with PCIe, PC/104 is on the brink of surpassing limitations and redefining its place in embedded computing. ➤



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